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Research on Automatic Measurement of Impulse Magnetic Noise (VI)

—Malfunction of Digital Circuit Caused by Electromagnetic Noise—

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Abstract

A jitter on a digital signal is one of the causes for malfunctions of digital circuit. It is thought that this jitter is generated by many kinds of noises. We designed a digital board which was composed of high speed CMOS logic ICs and exposed on it the external electromagnetic noises from an antenna. By the measurement of the frequency characteristics of a jitter appeared by it, the relations between the jitter and the appearance of a malfunction on a circuit is examined.

An electromagnetic wave has a sinusoidal waveform and its frequency is changed between the range of 20 to 200 MHz. As the results, it is found that the jitter has a few maximum and minimum values among the variation of electromagnetic frequency, and malfunction of the measured circuit appears on the discontinuous magnetic wave bands of the vicinity of the maximum values of the jitter.

Key Words: digital circuit, malfunction, external noise, jitter, CMOS logic IC

1. Introduction

At present, a design for timing on a digital circuit is determined on the foundation of the transmitting delay time caused by signal lines and digital ICs, and the mismatching reflection of the communicating lines. But on a practical circuit, it is happened that a few kinds of malfunction are appeared. It is supposed that some of the jitters are influenced by the cause of the jitters and glitch.

We accept that there are several causes in occurrence of the jitters and hazard. The researches of this problem are found in the following references.

For instant, Nishikata reported that a disturbing current by D.C.voltage gave an influence to a digital circuit. It is shown that as the results, a disturbing current of direct current causes to go out of order the timing of an action of the circuit which is composed of TTL-IC.

Also, we experimented about the next items. That is, we confirm that taking up a mutual inductance between the digital boards close to CMOS-IC, the noise voltage appeared by this mutual inductance causes to miss the timing of an action of the digital circuit.

In this experimental circuit a voltage signal caused by induced noise is capacitively superimposed on a digital signal.

In addition, the jitters which have the time width sufficient to cause the malfunction of a circuit by even the noise voltage of a smaller amplitude than the noise margin of CMOS-IC on

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the experimental digital circuit, was produced.

In this report, we explain about the results that we intentionally irradiate an electromagnetic wave on a digital circuit composed of CMOS-ICs and examine about the relations between the induced noises, jitters,and the malfunction of the circuit, and successively according to these results we discussed about the malfunctions of digital circuit by the induced noise.

2. Measurement Method

2-1. Experimental System

Fig.1 is the layout of an electronic circuit on the measuring board used at this experiment. Fig.2 is diagram of the electronic circuit. This circuit is constructed on a printed board made from glass epoxy (thickness:6mm). An electric source line, GND lines and signal lines are arranged on the one side of the board. Five inverters ICs:74 HCO4 (3/6)x1,(1/6)x4), an exclusive logic sum (74HC86), a CMOS digital IC of binary counter (74HC393) (all are DIP), and LED are arranged on the face. The capacitors, C and Ci, work as the loads. By changing these capacitive load a change of CMOS-IC on the next stage is able to be acted imitatively.

In this measurement, 33pF, 100pF, and 220pF are used as the capacitors Ci. This circuit is

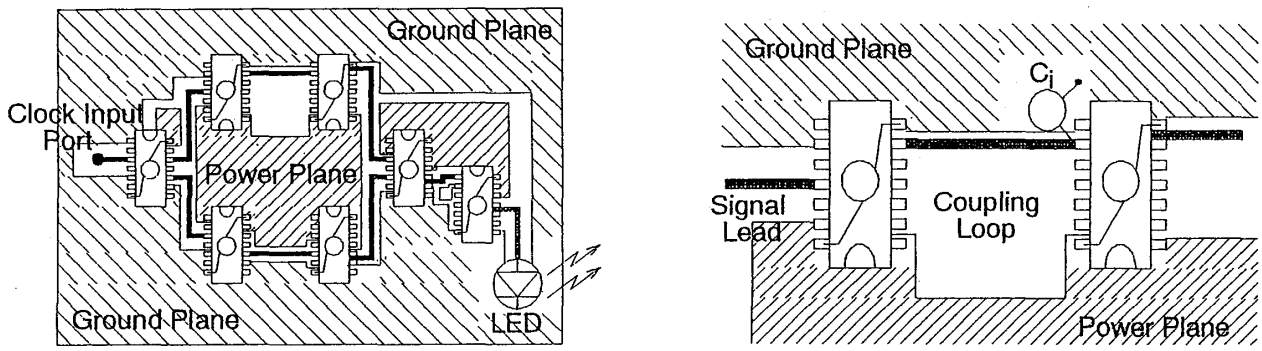

Fig.1 : Layout of the digital circuit board under the experiment ; whole view (A) and close-up near the loop area (B).

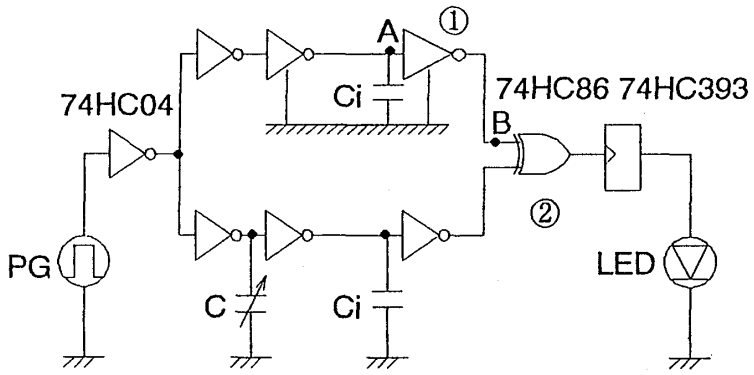

Fig.2 : Block diagram of tha wiring for the experiment.

divided into 2 systems consisted of the same circuit components each other. One of them has a layout in which forms a loop of 17mm x 17mm (area:289mm) with power supply pin, GND pin, power supply plane, GND plane and a part of signal line. This loop acts as a receiving antenna of radiated electromagnetic waves. The electromotive force occurs on this loop when electromagnetic waves are radiated on this circuit board.

This is an induced noise voltage superimposed upon the clock pulse running through a signal line. On the contrary, the another system is designed so as to have minimum area on a board, so that an influence of the irradiated electromagnetic wave make less. When a jitter occurs on an output of digital IC shown in Fig.2 ① by noise voltage superimposed on the first stage system, the glitches appear on the output signal of exclusive-OR at the next stage system. When these glitches have a time width enough to cause malfunction, the appearance of malfunction is indicated by the lighting of LED.

A loop antenna shown in Fig.3 is used as a radiation antenna. The specifications of a loop antenna are as follows.

Outside diameter of a coaxial cable : 2.2mmϕ
Inner diameter of a coaxial cable : 0.5mmϕ
coaxial cable : semirigid
diameter of loop formed by inner conductor : 16.2mmϕ

The antenna is matched by connecting 50 Ω resistance at the contact joint of loop. Signal tracer (HD8082) is connected with this loop antenna, and a sinusoidal voltage is applied to it. The amplitude of the applied sinusoidal voltage in this experiment is 2.4 V and its frequency, 20 to 200MHz. It is supposed that the electromagnetic intensity of 5mm fixed point in the normal direction of a loop antenna upon the measured board is 124 to 125 dBμA/m.

2-2. Experiments

All elements of the digital circuit under experiments are driven by a voltage level 3 V. A pulse generator inputs a square clock pulse voltage height and frequency are 3V and 4 MHz respectively to the circuit as a digital signal. At this conditon electromagnetic wave is irradiated on the board from the above-mentioned antenna. An antenna is fixed at the position where it holds the most closest inductance relation with a loop on the measured board as shown in

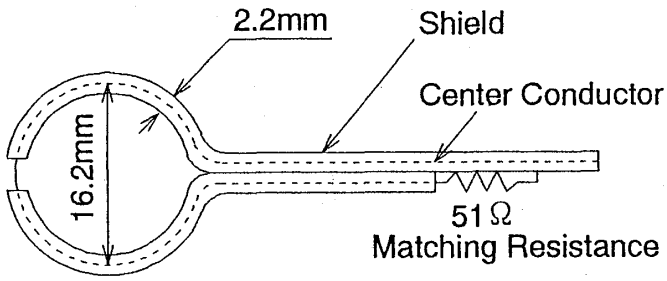

Fig.3 : Head part of the small loop antenna : This antenna is made of the 22mm diameter semirizid coaxial cable with split shield. The diameter of the loop is 16.2mm. A resisistor 51 ohm is for impedance matching.

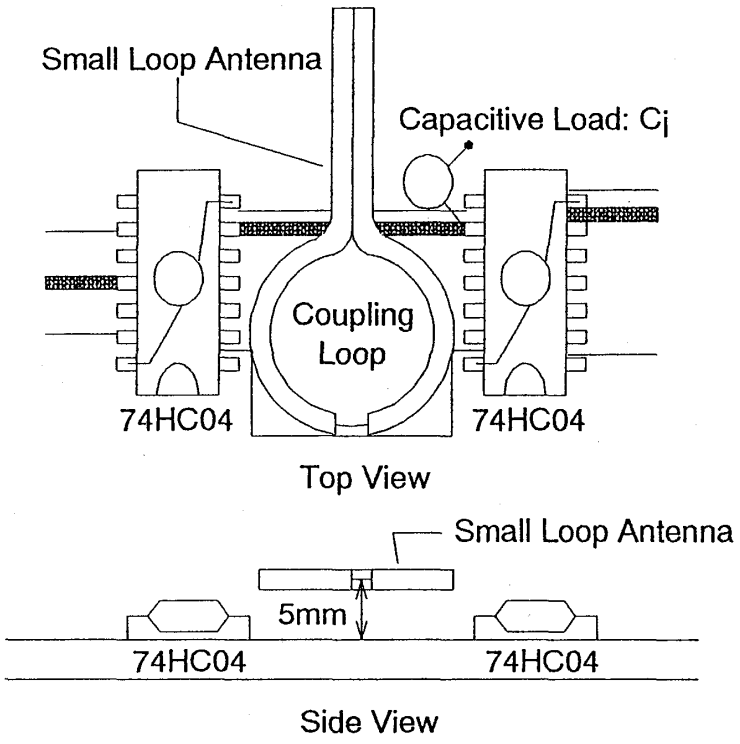

Fig.4 : During the experiments, the antenna and the circuit board are positioned 5mm apart. The magnitude of the magnetic field is presumed 124 to 125 dBμA/m at a distance of 5mm under the experimental condirion ; input amplitude 2.4V.

Fig.4. At this time the distance between the antenna and the board adopts 5 mm, and both hold parallel relation. A sinusoidal voltage of amplitude 2.4 V is applied to the antenna,and the frequency of a radiating field is changed by sweeping the frequency of a radiating field between the range of 20 to 200MHz at the intervals of 5MHz.

At this experiment, a shake of an input signal and a jitter of output signal at the gate of which the coupling loop is composed are measured, as well as the measurement of malfunctions occur. Digital oscilloscope (HP 54504A) is used in this measurement.

The two channels of A point of input side and B point of output side of gate were measured simultaneously. We estimated the maximum value of the swing width and jitter by applying the enveloping method (mechanism) for this measurement, because the measurement of instant swing width and jitter is impossible for accuracy limit of our measuring devices.

The measuring time is one minute. After this time, an enveloping curve became perfectly constant state. Terminals of these two proves for high frequencies are fixed tightly by using the jigs.

A width of swing is that which cuts down a voltage level width an envelope of step down part of input voltage at gate ①, and also, of a step-up of output voltage at gate ①. In this experiment, each widths of swing and jitter are measured, adopting a half voltage, 1.05V, of pulse height of voltage level, and threshold voltage, 1.37V (effective value) on gate ①.

3. Measuring Results and Discussions

3-1 Frequency at the Appearance of Malfunction and Jitter

Fig.5 shows that noise frequency domain at the time of malfunction of the measured circuit, and noise frequency characteristics of each jitters for two measuring voltage. By these data, it

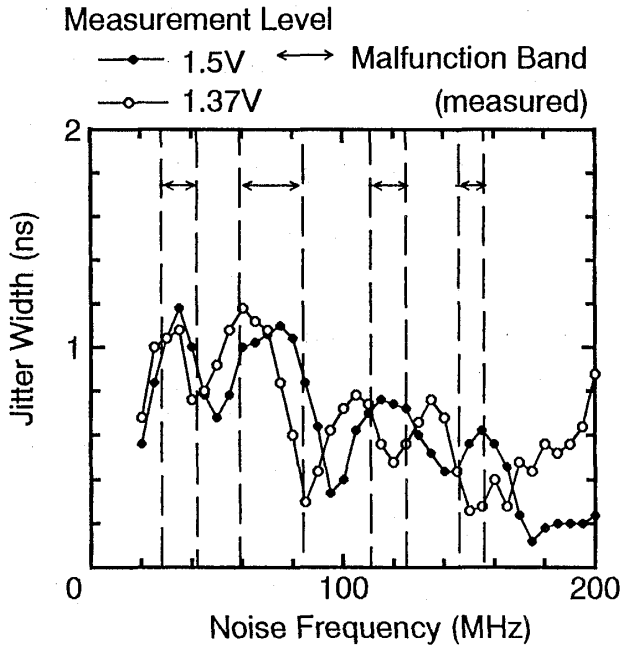

Fig.5 : Malfunction frequency bands and characteristic curves of the jitter width with a eapacitive load 220pF. The black circles are obtained at a measurement level 1.5V, and the white ones are at 1.37V.

is able to be understood that malfunction appears at noise frequencies in a discontinuous distribution state. Black circles show the jitters against various noise frequencies for the measurement at level, 1.50V of which clock pulse is half of maximum height, and white circles, the jitters measured at the threshold voltage, 1.37V of gate. Comparision between both cases, we found that noise frequencies which show maximal and minimal values shift according to the difference of measured voltage levels.

We think that this result is because jitters change according to transient parts of clock pulse. At present it is not obvious whether the fluctuation depends on voltage or time change. In comparison between frequency band distribution of malfunction on the measured circuit and noise frequency characteristics, we find that the noise frequency characteristics curves of jitter at the measured level, 1.50V are accord with the frequency bands which exceed the jitter width, about 0.6 nsec.

From these results, it is concluded that the jitters which appears at this voltage level is related to malfunction of a circuit. At present, we suppose it is appropriate to think that this voltage level is the threshold level of the digital IC at the next stage. It is supposed that the threshold level of exclusive logical summation (74HC86) is 1.50V, in the case of the measured circuit of this experiment. It is conceivable that malfunctions have appeared for a jitter of this level.

Fig.6 and Fig.7 are data which checked an influence by capacitive loads (100pF,33pF) at voltage level 1.50V. In comparison with the results of these 2 figures and the capacitive load (220pF) at Fig.5, we find that the frequency characteristics of jitter change, and the number of the poles decrease comparatively for a smaller capacitive load.

Next, the frequency bands of the malfunctions caused by the jitters shown in Fig.6 and Fig.7

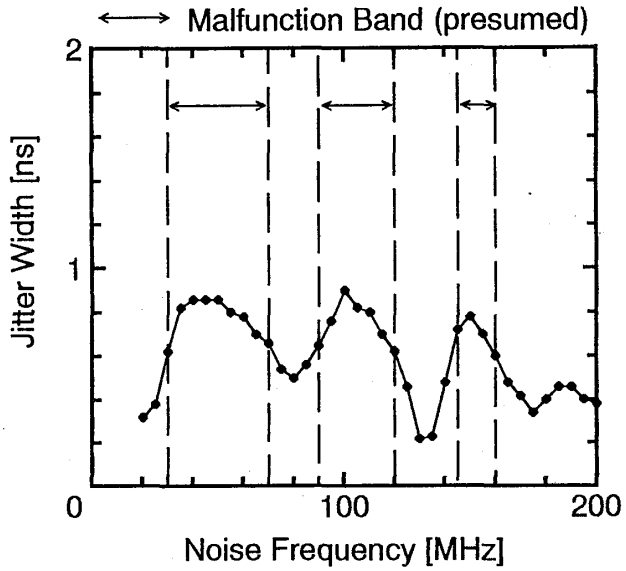

Fig.6 : Characteristic curve of the jitter width with a capacitive load 100pF. The malfunction frequency bands are presumed by the relationship between the characteristic curve at 1.5V and the malfunction bands shown in Fig.5.

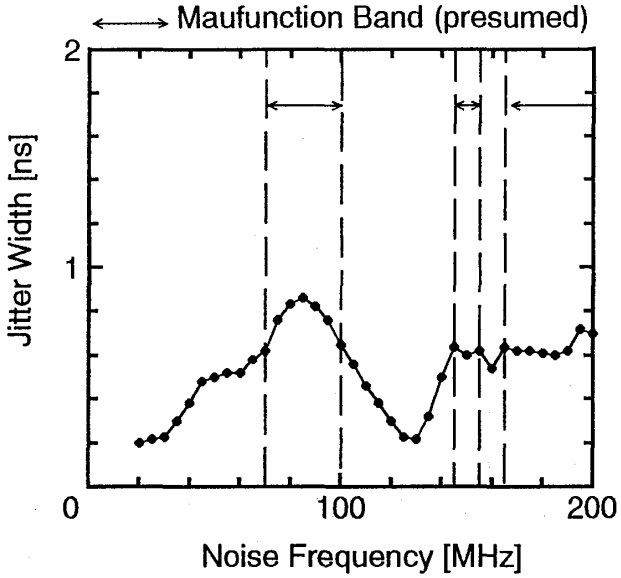

Fig.7 : Characteristic curve and the malfunction frequency bands with a capacitive load 33pF. The malfunction bands are obtained by the same procedure of Fig.6.

are are sectioned, and from these bands, we find trend that it moves toward higher harmonics, as a frequency band of malfunction becomes smaller.

3-2. Frequency Characteristics of Shaking Width and Superimposed Noises

According to our assumption of appearance of jitters, jitter width of the output should have a relation with the shaking width of the input at the same logic gate. The frequency characteristics of the jitters measured with a load capacity, 220pF, and shaking amplitudes are shown in Fig.8.

In this measurement, 1.37V, a threthhold level of input gate, is set up as a measured voltage level of a swinging amplitude, and 1.50V, as a estimated voltage level of an exclusive-or on a next stage. From this figure, we recognize that a pole in both of noise frequency characteristics and jitter appears, and also these noise frequencies agree with each other.

Fig.9 is one of the examples which show a clock pulse voltage on which a noise frequency of 200 MHz is superimposed. Using the envelope function for measurement, the noise causes contour of the wave form double. The width of this contour is 2 times as an amplitude of superimposed noise, but a transient part is influenced by an inclination of clock pulse. As the method by which the influence is made smaller, we measured the noise voltage by obtaining the difference from the basic clock voltage.

A noise voltage in each frequencies obtained by these operations is shown in Fig.10. The

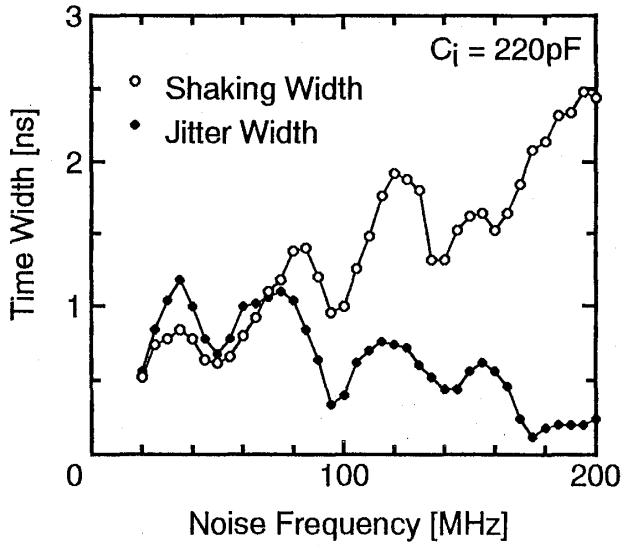

Fig.8 : Characteristic curves of the shaking and the jitter width for the same not-gate with a capacitive load 220pF. The 2white and the black circles show the shaking and the jitter width, respectively.

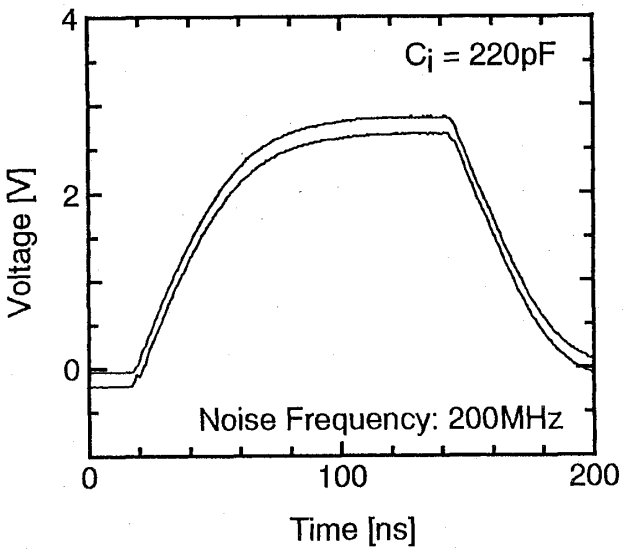

Fig.9 : The recorded clock pulse has the double contour because of the envelope function of the employed oscilloscope. The width corresponds to the peak-to-peak of the noise voltage along the wave form.

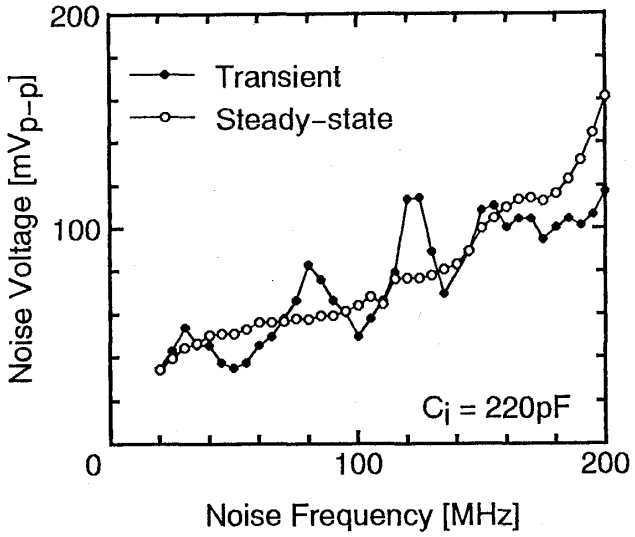

Fig.10 : Characteristic curves of the superimposed noise voltage at the steady-state and the transient part of the clock pulse with a capacitive load 220pF. The black and the white circles give the result at the steady-state and at the transient part, respectively.

black circles are the noise voltages in the transient part superimposed as a voltage level 1.37V, and the white marks, that of high level which is a steady state part on a clock pulse. The frequency characteristics of the noise voltage superimposed on a transient part is agreeing very well with a characteristics curve of the frequency of a swing width shown in Fig.8, and the noise frequency which gives a peak value, that of jitter. However, the noise frequency characteristics of a noise which superimposes on a steady state part has no peak values, and a noise voltage increases monotonously in proportion to a noise frequency. From these results, it is found that a jitter of an output is decided by the noise which is superimposed on a transient part.

From the results of the aforementioned investigations, it is concluded that each of the appearances of the noises are different for a transient action state and steady state of digital CMOS-IC. In Fig.10, the peak values of the voltage of the superimposed noises on the transient parts are found to be larger than the noise voltage on a steady state part at the same frequency.

These facts show that a larger noise than the superimposed noises at the steady state of a CMOS digital IC is superimposed on IC input signal at the transient action, and moreover, it is difficult that this amplitude can be easily predicted, even if the size of the superimposed noise at the steady state can be known. The reason why the difference of the response characteristics between the noise in a transient part and steady state part of a clock pulse occurs can not be confirmed yet. But it is supposed that a change of parameters in circuit by a transient action of CMOS-IC is one of the causes.

A general idea of this expectation is able to confirmed from the superimposed noise voltage on a clock pulse. An envelope line of 200 MHz superimposed on a clock pulse is shown in Fig11(a) and Fig.11(b), adopting time as the axis of abscissa.

Fig.11(a) shows an enveloping line of steady state which does not change according to time, and in Fig.11(b) a width of enveloping line of the transient part changes cyclically according to time.

Fig.12 and Fig.13 show an envelope line state of the transient part of a clock pulse at the superimposed frequencies, 150 MHz and 100 MHz.

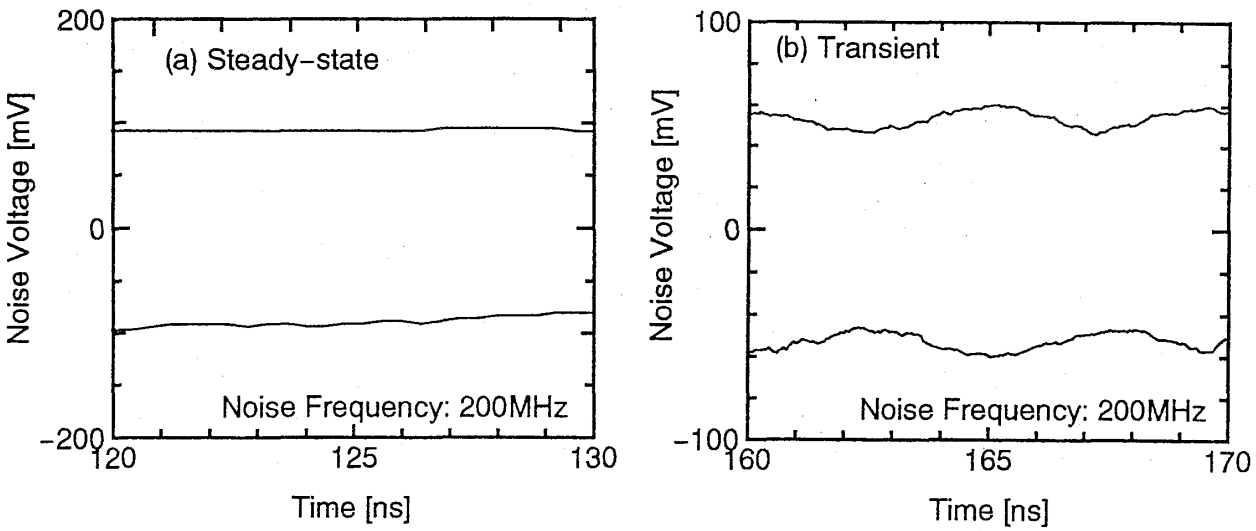

Fig.11 : Close-up of the double contours at a part of the steady-state (a) and of the transient (b) at a noise frequency 220MHz : They are obtained by subtracting the clock pulse products from the raw data. Their width can give the real peak-to-peak voltage of superimposed noise. The contour at the transient part has the periodic fluctuation, which is not found at the steady-state part.

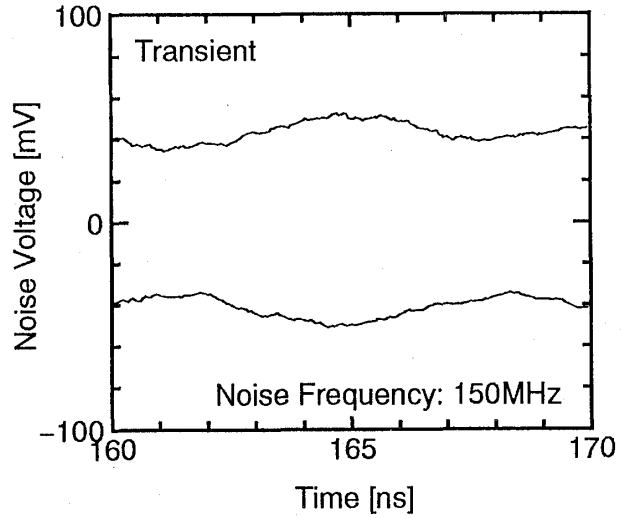

Fig.12 : Double contour at a part of the transient of the clock at a noise frequency 150MHz.

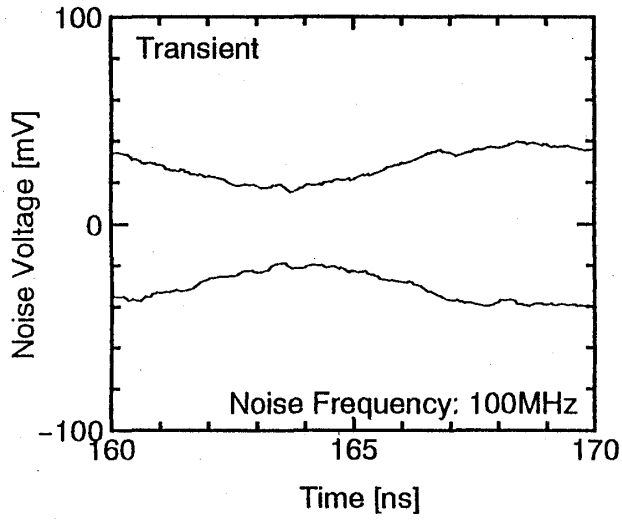

Fig.13 : Double contour at the transient part of the clock at a noise frequency 100MHz. Comparing this result with the results of Fig.11 (b) and Fig.12, it is found that each fluctuating period of the contour corresponds to a frequency of the superimposed noise.

This noise voltage has such a periodical fluctuation as in the case of Fig.11(b). It attracts our attention that the period is equal to one of each superimposed noises. As it should show an envelope line of the same width on a transient and steady-state part on our experimental system, it is supposed that an occurrence of this fluctuation depends on the continuous change of circuit parameters in loop of a experimental system.

4. Conclusion

A relationship between the appearance mechanism of the jitter on the clock pulse by a radiated electromagnetic wave and malfunction of circuit was researched. In this experiments,

by radiating an electromagnetic wave on a digital circuit we measured the noise voltage superimposed on clock pulse voltage, shaking width, jitter width and also the frequency of appearing malfunctions.

As the results we found that malfunctions of a circuit appeared in four discontinous bands of the noise frequency, and these bands located close to noise frequencies which gives maximal jitter widths.

It was made clear that one of the causes of its appearance is the deterioration of an immunity of digital circuit against a specific frequency of noise, and malfunctions of a circuit have the deep relations with a jitter width in a proper threthold level of IC. In addition, a maximum value of a jitter is about 1.2 nsec when the amplitude of a noise voltage is about 30 mV.

In comparison between noise frequency characteristics of a jitter width and swing amplitude which are a cause of malfunctions, both of noise frequencies almost agree with in peak and bottom values.

We also find that a noise frequency characteristics of the amplitude of the noise voltage that generates a shaking phenomena in a steady state part (HI level) differ from that in transient part (drop down part) of a clock pulse voltage. Especially, the maximal amplitude of the superimposed noises on a transient part is different perfectly with that of a transient part. The amplitude of the superimposed noise at a transient part is larger than that at a steady state part.

These mean that, namely, an immunity of a circuit from a noise differs with each cases of a steady state and transient state of digital IC. Especially, these facts become a important problem in the case of an immunity of a digital circuit at a high speed operation.

Furthermore, we found that from the noise voltage superimposed on a clock pulse, the amplitude of the noise superimposed on a transient part changes with a period of incident noise. At present, a cause of the occurrence of the phenomenon is unable to be made clear. We suppose that circuit parameters on high frequency loops are changed by the transient action of CMOS-IC. For instance, a resonance of high frequency loop will be one of the causes of the phenomenon. At this time, there is a undesirable possibility that the malfunction of very difficult supposition may occur by the appearance of digital signal which has a jitter width differing with various loops distributed between digital circuits.

From now on, we will examine the relation between the timing of a clock pulse voltage and a decrease of an immunity of a digital circuit by the noise coming from environment.

Furthermore, we schedule to research to clarify the relation of the resonance characteristics of high frequency loops and the superimposed noise voltage, and the malfunctions of a circuit by an connection between print circuit boards.

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